# ELLIOTT 900

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Part 3: OPTIONAL UNITS

Section 2: NPL INTERFACE MATCHING UNIT

CONTENTS





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END-OF-TEXT FIGURES



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# Chapter 1: GENERAL

## 1.1 Introduction

The 900/NPL Interface Matching Unit is designed so that peripheral devices having an NPL interface can be used with the 900 system. The IMU can be connected to the central processor via the general peripheral socket or via a multiplexer.

The IMU can be provided with facilities for up to 4 devices to be used. When only one interface is required, a master interface is supplied. When 2, 3, or 4 interfaces are required, a master interface and 1, 2, or 3 slave interfaces are supplied.

The IMU is a self contained unit which can be housed on three shelves of a standard 900 desk. The layout of the unit is shown in Figure 1. The master or slave interface logic consists of 4 boards per channel, giving a maximum of 16 boards for a 4 channel IMU.

Additional information can be obtained from Sections 1.2.7, 900 Standard Peripheral Interface and 1.3.2., NPL Interface Matching Unit.

## 1.2 Connections

Each interface channel has two cables connecting the device to the IMU. One cable carries input data and control signals, the other cable carries output data and control signals.

The IMU is connected to the central processor via two cables. One cable carries input and output data and control signals, the second cable carries control signals only.

The plugs and sockets associated with the IMU are mounted on an entry panel as shown in Figure 1.

## 1.3 Logic Drawings

The circuits of the L. S. A. elements used on the logic boards are described in Section 4.1.1. The tables in Figure 5 provide details of the types of L. S. A. element on each board and the location and value of any extra components used.

On the logic diagrams, Figures 3, 4 and 6, signals to and from the central processor are enclosed in square brackets [ ] and signals to and from the peripheral devices are enclosed in diamond brackets < >. All discrete components, not being part of the logic sub-assemblies, are fitted in Area G of the logic board.

# Chapter 2: POWER SUPPLIES

## 2.1 Introduction

The power supply equipment occupies one rack of the IMU assembly. The d.c. supplies are provided by three separate proprietary units. Details of these can be obtained from the manufacturers handbooks. A mains filter unit and a d.c. over-voltage protection circuit are also incorporated. The relative positions of the units in the rack can be seen in Figure 1.

## 2.2 D.C. Supplies

The d.c. supplies required by the logic boards are +6 Volts, -6 Volts and +12 Volts. The +6 Volts is provided by PU1, Catalogue No.11258, the output line being fused at 3A. The -6 Volts is provided by PU2, Catalogue No.11258, the output line being fused at 1A. The +12 Volts is provided by PU3, Catalogue No.11186, at a current rating of 1A. Figure 2 shows the connections within the power chassis and the distribution of the d.c. supplies to the logic rack.

## 2.3 Over-Voltage Protection

An over-voltage protection circuit is connected across the +6 Volts and -6 Volts d.c. outputs to protect the logic boards from damage due to a rise in level of either of these supplies. Under normal operating conditions, no current is taken by the circuit.

If either of the d.c. outputs start to rise then current will be drawn through the corresponding zener diode and current applied to the thyristor. Dependent on the ambient temperature and component tolerances, the thyristor will be triggered when the d.c. level has risen to a value between 6.5 Volts and 10.0 Volts.

When the thyristor conducts, the output terminals of the power unit are short circuited causing the appropriate fuse to blow.

# Chapter 3: LOGIC DESCRIPTION

## 3.1 Introduction

This chapter contains a functional description of the control logic associated with the 900/NPL Interface Matching Unit when used to transfer data in either direction between a peripheral device and the central processor. The unit consists of a master and up to three slave interfaces, each contained on four logic boards. The logic rack is wired to accommodate the maximum of four interfaces, so that a 1, 2 or 3 channel unit can be expanded, by the addition of the required slave interface logic boards.

## 3.2 Master and Slave Interfaces

The master interface contains the main address decode logic, the data transmitters and the data receivers which are used by both master and slave interfaces. In other ways the slave interfaces behave logically in a similar manner to the master interface.

The master interface logic is shown in Figure 3 and the slave 1 interface logic in Figure 4. The changes in signal names and plug and socket numbering required so that Figure 4 can be used for the slave 2 and 3 interfaces, are quoted in round brackets ( ) where appropriate after the slave 1 annotations. The logic description in this chapter applies to the master interface.

## 3.3 Address Decode

The selection of the IMU and the particular channel required is determined by the state of the signals [OS8] to [OS11], [OS1] and [OS2] from the central processor. For the IMU to be addressed then [OS8] to [OS11] must all be false. The particular channel required is determined by the state of [OS1] and [OS2].

The main address decode of signals [OS8] to [OS11] is carried out by 16/1B11, 16/1B12, 16/1B13 and 16/2B11, the outputs being linked together. When all inputs are false a true signal is obtained, which is inverted by 16/2A11.

When the processor requires to output via the IMU, the interface signal [SOP] is made true. This signal is inverted by 16/3B12 and gated with the output of 16/2A11 at 16/3A11 and 16/3A12, causing ADDRESS* to go true.

When an input is required to the processor, the interface signal [SIP] is made true. This signal is inverted by 16/3B11 and gated with the output of 16/2A11 at 16/1A11 and 16/1A12, causing ADDRESS 1 to go true.

The channel selection signals [OS1] and [OS2] are inverted by 16/2B12 and 16/2B13 to produce $\overline{OS2}$ and $\overline{OS1}$ respectively. A further inversion by 16/2A12 and 16/2A13 produces OS2* and OS1* respectively. ADDRESS 1 or ADDRESS* and any two of the signals derived from [OS1] and [OS2] are gated such that only one interface responds to an input or output demand signal from the processor. The interfaces are selected as follows:-

(1) Master interface selected when [OS1] and [OS2] false.

(2) Slave 1 interface selected when [OS1] true and [OS2] false.

(3) Slave 2 interface selected when [OS1] false and [OS2] true.

(4) Slave 3 interface selected when [OS1] and [OS2] are true.

### 3.4 Data Output Buffering

The output buffering logic is located on board type DP103 in position 15 of the logic rack and consists of eight identical lines. Each 900 interface data line [OA1] to [OA8] is buffered by a receiver 15/1B11, 15/1B12 etc. The data signals $\overline{\text{DATA11}}$ to $\overline{\text{DATA18}}$ are then distributed to the special transmitters in each of the interface channels. The transmitters are designed to meet the requirements for the NPL interface. The device selected by the processor will then accept the data from the lines.

### 3.5 Data Input Gating

The input gating logic on board type DP101 in position 17 of the logic rack, contains eight logically identical data lines. Taking <DATA1/0> as a typical example, the signal from the peripheral is buffered by a special receiver 17/1B11, designed to meet the requirements of the interface, the element also inverts the signal. After a further inversion at 17/1A11 the signal is gated with SIP.0 at 17/4A11 to produce $\overline{\text{DATA1}}$ and transmitted to the central processor as [IG1] by 17/4B11. The gated data signals from the slave interfaces are also routed to the processor via the transmitters on this board.

### 3.6 Data Output Transfer

When data is to be output from the processor to a peripheral device, [SOP] is made true and, as described in para.3.3, causes ADDRESS* to go true. Assume that the master interface is selected and [OS1] and [OS2] are false, therefore $\overline{\text{OS1}}$ and $\overline{\text{OS2}}$ are true.

ADDRESS*, $\overline{\text{OS1}}$ and $\overline{\text{OS2}}$ are gated at 16/7B13 causing its output to go false. The false signal is inverted by 16/6B12 and 16/6B13 causing $\overline{\text{JS0}}$ to go false. A further inversion by the transmitter 15/7B11 causes

<JS0> to go true. This signal is fed to the peripheral device, and when it goes true, causes the device to accept the data output from the central processor. When the device goes busy, it makes <KS0> false.

After the data has been accepted by the device <KS0> goes true. <KS0> is applied to the element 16/4B11 which introduces a 100 μs delay before its output is at the level required to operate the Schmidt trigger circuit of 16/5B13. When the Schmidt circuit operates, the output of 16/5B13 goes false to trigger the pulse generator 16/4A13. The resultant pulse is inverted by 16/5A12 and used to set the bistable 16/5A13, 16/7B11 causing $\overline{\text{SET REPLY0}}$ to go false. This signal fed to 14/5B12 causes a true [PR] signal to be sent to the central processor from the transmitter 14/7B11.

After a short delay the processor makes [SOP] false. This causes ADDRESS* to go false, the output of 16/7B13 to go true and <JS0> to go false. The output of 16/7B13 is inverted by 16/1A13 to produce a false signal to reset the bistable 16/7B11, 16/5A13 causing $\overline{\text{SET REPLY 0}}$ to go true and [PR] false. It is a requirement of the NPL interface specification that <JS0> remains false for at least 10 μs every time that it goes false. The monostable, formed by 16/6A13 and 16/6B11, is triggered when the output of 16/6B12 goes false and holds this point, and therefore, <JS0>, false for the required 10 μs period.

## 3.7 Data Input Transfer

When an NPL peripheral device has data available for transfer to the central processor, it makes the <JP0> line true.

The <JP0> signal is applied to the delay element 14/3B11, the output of which controls the operation of Schmidt trigger 14/4B13. When

<JP0> goes true, a delay of 100 μs is introduced before the output of the Schmidt trigger circuit goes false. The negative-going edge causes the pulse generator 14/4A13 to produce a 1 μs pulse. The pulse is inverted by 14/3A11 and sets the bistable 14/2A13, 14/2A11 such that the output of 14/2A11 is true. Interface signal [SIP] is false, holding ADDRESS 1 false and $\overline{\text{SIP.0}}$ true. This signal is gated with the output of the bistable element 14/2A11 at 14/2B12 and when the bistable is set, causes $\overline{\text{INTERRUPT.0}}$ to go false.

The output of bistable element 14/2A13 goes false when the bistable is set and via 14/5B11 and 17/7B12 causes <KP0> to go false.

The interrupt signals from the four channels are connected to terminals NPL1 to NPL4 on a patch panel mounted in the logic rack. By means of jumper connections the interrupts can be connected to any one of the peripheral interrupt lines to the central processor. These lines PI1, PI2 and PI3 are accessible via terminals 1, 2 and 3 respectively.

When a PI line goes true, it causes the computer to jump to a routine calling for an input from the device which originated the interrupt signal. Interface signal [SIP] is made true with the following results:-

(1) Via the logic elements 16/3B11 and 16/1A12 ADDRESS 1 is made true. With the master interface selected $\overline{\text{OS1}}$ and $\overline{\text{OS2}}$ are true and $\overline{\text{SIP.0}}$, the output of 17/7B11, goes false. This signal closes the gate 14/2B12 causing $\overline{\text{INTERRUPT.0}}$ to go true.

(2) $\overline{\text{SIP.0}}$ is inverted by 17/6A13 and gates the information from the peripheral device, <DATA1/0> to <DATA8/0>, onto the processor input lines [IG1] to [IG8].

(3) $\overline{\text{SIP.0}}$ is inverted by 14/1B12 and gated with the true output of the bistable element 14/2A11 at 14/2B11. The resultant negative signal triggers the pulse generator 14/7A13, which produces a 10 μs pulse. At the end of this pulse, a second pulse generator 14/5A13 is triggered. The 1 μs pulse produced is inverted by 14/2B13 and sets the bistable 14/3A12, 14/3A13 causing the output of 14/3A13 to go false. This results in [PR] going true via elements 14/5B12, 14/5B13 and 14/7B11.

After receiving the true [PR] signal, the processor inputs the data present on the lines [IG1] to [IG8] and then makes [SIP] false. This results in $\overline{\text{SIP.0}}$ going true to perform the following functions.

(1) $\overline{\text{SIP.0}}$ is inverted by 14/1B11 and triggers the pulse generator 14/1A13. The 1 μs pulse is inverted by 14/1B13 and used to reset the bistables 14/2A13, 14/2A11 and 14/6B12, 14/6B11.

(2) The output of 14/1B11 is also used to reset the bistable 14/3A12, 14/3A13 causing [PR] to go true.

(3) The bistable 14/2A13, 14/2A11 being reset causes the output of 14/2A13 to go true and hence <KP0> goes true.

## 3.8 Reset Signals

To ensure that all bistables are set to the correct state, when the equipment is switched on, a [RESET] signal is employed. This is obtained from the central processor and is at a true level when the equipment is first switched on and also when the Reset button is operated. The signal remains true until the Jump button is pressed.

For the input interface logic it is essential to set the bistable 14/2A13, 14/2A11 according to the logic state of <JP0>. When the [RESET] line is true $\overline{\text{RESET 0}}$* is false and the bistable 14/6B11, 14/6B12 is reset so that the output of 14/6B11 is true. This true signal is gated with the output of the Schmidt trigger 14/4B13 at 14/6A13 and with the inverse of the 14/4B13 output at 14/6A12. This results in the output of 14/2A11 being set true if <JP0> is true and set false if <JP0> is false.

The bistable 14/6B11, 14/6B12 is reset at the end of the first data input transfer when [SIP] goes false, and thereafter the bistable 14/2A11, 14/2A13 is only set when the <JP0> signal goes true.

$\overline{\text{RESET 0}}$* being false and applied to 14/5B11 ensures that the output of 15/7B12 is held false and the peripheral device does not receive a spurious <KP0> pulse.

In the output interface logic $\overline{\text{RESET 0}}$* going false resets the bistable 16/7B11, 16/5A13 such that $\overline{\text{SET REPLY 0}}$ is true and hence [PR] is false.

RESET*, the output of 16/3A13, is fed to the slave interfaces to provide the reset conditions.

# Chapter 4: STATUS WORD FACILITY

## 4.1 Introduction

The status word is an optional facility which may be employed when more than one channel of the IMU is used. Under normal conditions, the interrupt signals generated when a peripheral device has data ready to transfer, are routed to the central processor on separate lines [PI1], [PI2] and [PI3].

When the status word facility is included, the interrupt signals are commoned onto one line. On receipt of an interrupt signal, the processor enters a routine which inputs the status word via interface lines [IG1] to [IG4]. These signals are true when a peripheral has data ready for transfer. [IG1] corresponds to the master interface, [IG2] corresponds to slave 1 etc.

The logic for the status word facility is on a type DP108 board and is inserted in position 18 of the logic rack.

## 4.2 Status Word Logic

The logic diagram of the board is shown in Figure 6.

On receipt of an interrupt signal, the processor inputs the status word to determine which peripheral channel originated the interrupt. [OS5] and [SIP] go true and [OS8] to [OS11] inclusive remain false.

[OS5] is fed to board 18 where it is inverted by 18/1B11 and 18/2B11 and causes ADDRESS 1, the output of 18/3B11, to go false. This signal fed to board 16 pin 38 inhibits the gates 17/7B11, 13/7B11 etc. ensuring that the data gating signals $\overline{\text{SIP0}}$, $\overline{\text{SIP1}}$ etc. are not generated.

$\overline{\text{SIP}}$ and $\overline{\text{OS8/11}}$ derived from board 16 are inverted by 18/2B13 and 18/2B12 respectively. The common output is gated at 18/3B12 with the true signal derived from [OS5] causing the output of 18/3B13 to go true. This true signal is fed to the three gates of element 18/4B and to 18/5B11.

The interrupt signal is generated by a peripheral making its <JP0> line true. As described in Para. 3.7 this causes $\overline{\text{INTERRUPT 0}}$ to go false and $\overline{\text{KP0}}$ the output of 14/5B11 to go true. The $\overline{\text{KP0}}$, $\overline{\text{KP1}}$ etc. signals are fed to the three gates of element 18/4B and to 18/5B11, the signals that are true causing the outputs of the gates to go false. These signals $\overline{\text{DATA 1}}$ to $\overline{\text{DATA 4}}$ are fed to the transmitters on board 17 and hence onto the interface lines [IG1] to [IG4].

For normal data input transfers, [OS5] is false causing ADDRESS 1 and $\overline{\text{DATA 1}}$ to $\overline{\text{DATA 4}}$ from board 18 to be true. This allows data from the peripheral to pass to the interface lines as described in Chapter 3.